Wafer Backside Processing (WBP) without Frontside Protection for Etching of Nitride- and Polysilicon-Layers and Damage-Removal

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Introduction

1) Wafer Backside Etching: In the semiconductor production sequence some processes are used which deposit layers simultaneously on the wafer frontside and backside. Examples are oxidation- (thermal oxide) and CVD-processes (doped and undoped polysilicon, silicon oxide, silicon nitride). Since a (sandwich) layer on the wafer backside is not always beneficial (i.e. reproducibility problems of temperature measurement during RTP-processes), these layers have to be removed periodically.

Current approaches use a frontside protection consisting of photoresist. The layers on the backside are removed by a wet chemical dip or an isotropic CDE dry etch step (Chemical Downstream Etching). Following the backside etch the photoresist protection on the wafer frontside has to be removed. This sequence with the (additional) photoresist coating and stripping steps shows a long cycle time, requires equipment capacity (PR-coater, stripper, and cleaner), represents a contamination risk, and consumes a significant amount of chemicals (environmental pollution problems).

To avoid these problems, a wet chemical approach without frontside protection has been introduced by SEZ [1]. The frontside of the wafer is placed upside down on the air cushion provided by a specially designed chuck. While the chuck with the wafer is rotating at high speed, the wet chemical etchants are sprayed onto the backside. Due to the rotation the etchants move to the wafer edge and are flinged off without contacting the wafer frontside. This approach is meanwhile established on the world market, but shows, nevertheless, some drawbacks. The consumption of chemicals including the DI-water for the water rinse causes high costs and is critical in terms of disposal. Furthermore, the nitride etch rate is very slow compared to the high polysilicon and oxide etch rate. Considering all these facts, a new method of backside removal seems to be desirable.

2) Damage Removal: After thinning finished silicon wafers, their backside have a disturbed, compressive stress causing surface, which is - especially in the case of very thinly grinded wafers (e. g. chip card applications) - removed with a wet process (damage etching). This is connected with a high consumption of chemicals and DI-water and, in the case of a spin etcher, also with very delicate handling for thin wafers.

Therefore, a process based on microwave-supported downstream etching was developed, which works without wet chemistry and allows gentle manipulation. Regarding results (bow removal, breaking strength), the process is comparable to wet processes and because of the minimal media consumption, cheaper than competing wet processes.

Principle of New Approach

The new approach [2] has been developed in cooperation with the Austrian equipment supplier SECON. It is based on chemical downstream etching with a high yield radical generator based on the SEMWAVE technology [3] without additional frontside protection on the wafer.

The substrate is transported and placed in the etch chamber in the normal mode (frontside up). The radical generator is mounted at the bottom of the chamber (see Fig.1). According to normal CDE, the radicals diffuse to the substrate and react there. The etch products are pumped off via a ringshaped slit above the wafer edge.

The frontside of the wafer is protected non invasivly by a neutral gas. The neutral gas flow, which suppresses the diffusion of the reactive radicals to the frontside, is maintained by a special design of the chamber head. Due to this design, it is possible to etch in different modes. Often it is beneficial to remove layers not only from the wafer backside. Etching the rim of the wafer and a small but sharply defined region on the wafer edge on the frontside (edge exclusion) can avoid cracking or popping on these areas (better contamination control)

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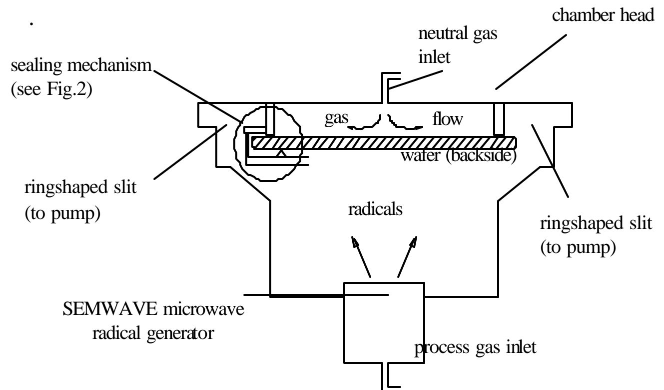


Fig. 1: Principle chamber design

The edge exclusion can be realized by use of a special sealing mechanism (Fig.2). After the wafer is placed to a movable chuck (the spider), the chuck moves towards the upper sealing. The spider is stopped by an indirect stop outside the area reserved for the wafer. With a correct adjustment of the stop, the distance betwen sealing and wafer frontside is ≤ 0.1 ± 0.01 mm.

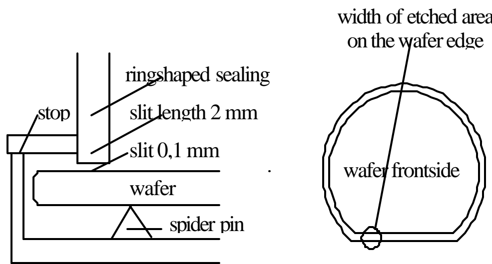


Fig. 2: Priciple of the sealing mechanism

Applying a slight overpressure of the neutral gas within the sealing, a constant gas flow towards the sealing can be maintained. This gas flow prevents a penetration of the reactive radicals but is not strong enough to influence the process on the wafer backside and the defined wafer edge areas. The pressure difference between the etch and the neutral (protection) gas influences strongly the transition region betwen etched and unetched regions under the sealing. It is, therefore, an important parameter to adjust a sharp transition between these regions. With an optimized setup, a transition length smaller than 0.2 mm can be obtained which means that the transition looks optically very sharp. Using an optimized six pin spider, the regions under the pins can be etched residue-free.

The backside etch chamber itself is attached to a MESC-compatible cluster tool (IRIDIUM) also built by SECON (Fig. 3). It consists of two ports for load/unload stations, and ports for up to four process chambers. For the experimets a 150 mm version of the tool has been used, but also 125 and 200 mm versions are available.

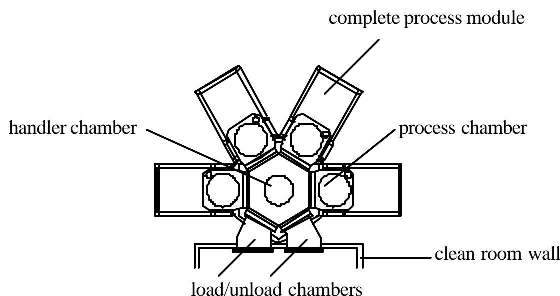


Fig. 3 : Schematics of the IRIDIUM backside etcher

Application for
Nitride Removal before Field Oxidation

One interesting application for the new tool is the stripping of the PBL-mask (Poly-Buffered-LOCOS) from the wafer backside before field oxidation. Stripping before the LOCOS-process is beneficial, because the wafer backside will be oxidized as well and protected against contamination this way. For this application a SF_6/N_2O etch process with a LPCVD-nitride etch rate of 300 nm/min, a polysilicon etch rate of 1000 nm/min, a thermal oxide etch rate of 10 nm/min, and a uniformity of ± 5 % has been developed. The nitride/oxide selectivity is 30. If this selectivity is not sufficient, some percentages of chlorine can be added to the process. Depending on the chlorine flow, selectivities up to 100 can be achieved as well. For a sandwich of 150 nm nitride and 150 nm polysilicon, the throughput of a system with two etch chambers is more than 40 wafers/h, and for 250 nm nitride on 250 nm polysilicon more than 30 wafers/h.

Table 1 : Comparison of standard, SEZ and WBP (Wafer Backside Processing) process flow

	Std.	SEZ	WBP
Nitride/poly-deposition and LOCOS-litho	x	x	x
Patterning of LOCOS-nitride on frontside	x	x	x
PR-strip in O_2-plasma	x	x	x
Cleaning	x	x	x
Protection coating on frontside	x		
Nitride/poly backside etch	x	x	x
PR-strip	x		
Cleaning	x		

Table 1 shows a process sequence with normal frontside protection, with the SEZ-method, and with the new WBP-method (Wafer Backside Processing). With the WBP- and the SEZ-approach, it is possible to get rid of three additional process steps. The gain in cycle time is several hours. Unfortunately, the SEZ etch process is very expensive due to inefficient use of wet chemistry. In comparison, the new WBP-approach shows high throughput and low consumption of chemistry (gases). The costs are a fraction compared to both other methods.

Application for
Simultaneous Etch of Both Wafer Sides

For some applications it is necessary to etch frontside and backside of the wafer simultaneously. This also can be done in the WBP chamber. In this case the spider remains in loading position (no movement to the stop) and no neutral gas flow is turned on. Contrary to existing CDE frontside etching systems, the wafer backside clears slightly before the frontside is finished. This is beneficial because the overetch can be adjusted specifically to the requirements on the wafer frontside.

The new system enables furthermore the important option to perform a two-step process with a backside etch only in the first step, and an etch of both sides in the second step. This may be necessary incase of a more sophisticated application where the frontside nitride is already thinned distinctively by a CMP-step.

If the WBP-chamber should only be used for backside etching, it is possible to etch the frontside sequentially in a standard Secon-CDE-chamber on the same tool (see Fig. 3).

Application for Damage Removal on Mechanically Thinned Wafers

At the end of the manufacturing process of silicon wafers with semiconductor elements, wafers are thinned and then cut into single chips. This thinning process leaves a disturbed, stressed silicon surface on the backside. When the wafers are extremly thin (e. g. for chip card applications < 200 µm), they can break during handling (final wafer testing, transport, dicing, ...) or during subsequent bendtests because of this stress.

To prevent uncontrolled breaking, the backside is etched a few micrometers in a wet etch system, in order to remove the stress-causing damage zone. The wafer frontside is protected by a thick (~ 100 µm) foil, which is applied for its protection already before the backside grinding process

Next to dip-etching, which is suitable only for small throughputs, a spinetcher is being used more and more. In this process, silicon wafers are clamped onto a rotating chuck with the face down. Between chuck and wafer, air flows radially outwards, while the wet chemistry is sprayed from above onto the wafer backside. Due to the fast rotation and the air cushion of the wafer, the chemicals are spinned outwards over the edge of the wafer backside and thus cannot attack the frontside. This process works considerably better than dip-etching, but has also several disadvantages :

- high consumption of wet chemicals and DI-water
- supply being available and controlled disposal of media
- intricate waferhandling with danger of breakage of very thin wafers
- the protective foil practically has to be removed before the etch process, since it can lift off the wafer in the region of the clampfinger, and thus etch liquid can get in between.

On the other hand, it would be desirable to leave the foil on until after the etch process, as it would hold the wafer fragments together in case of breakage, and thus make the cleaning more simple.

A dry removal of the damage layer was investigated by using gentle, microwave-excited chemical downstream processes with fluorine compounds.

Etching of silicon on the wafer backside can be done with CF_4/O_2-chemistry as well as NF_3- oder $SF_6/O_2/N_2$(or N_2O)-chemistry. Since etching is done preferably on damaged locations or along stresslines, respectively, only a short etchtime is necessary (depending on the thinning process and etch chemistry between 10 sec and 2 min), to remove the stress from the wafers. This can be checked with measuring the bow.

Controlled overetch rounds the tension cracks in the substrate at their ends so that the required breaking strength is obtained. SEM examinations show that the surface changes considerably already after 15 sec NF_3 microwave plasma. After longer etch times, deeper trenches are leveled, whereby their appearance strongly depends on the etch chemistry used. Contours will be softest with a SF_6-chemistry, while a certain roughness will remain with NF_3- und CF_4-chemistry and trenches caused by more severe damages will even show anisotropic contours. The etch rate with NF_3-chemistry is ≈ 1 µm/min, and ≈ 0,5 µm/min with SF_6- and CF_4-chemistry, respectively.

On grinder-thinned wafers, the bow disappears already after 10 sec of NF_3-microwave plasma. The decrease of the bow is proportional to the etch time.

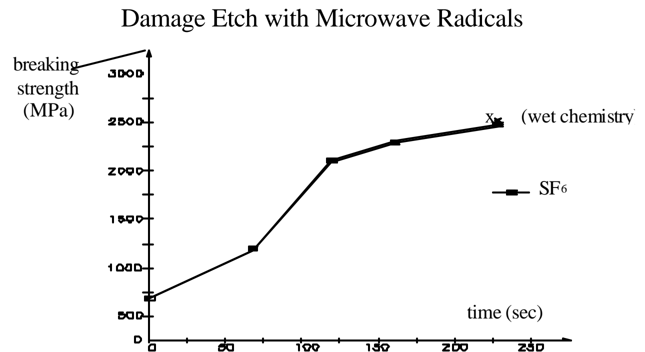
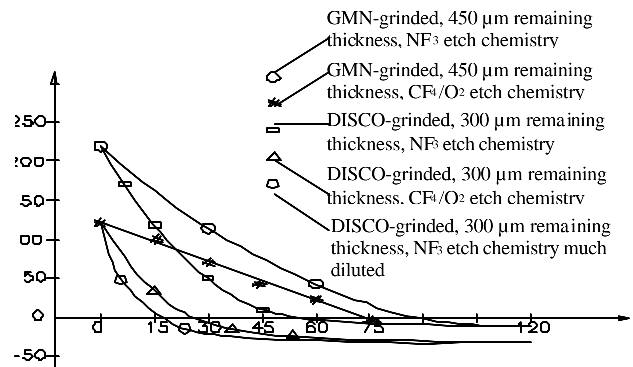


Fig.4: Breaking Stress in Dependence of Etching Time

For testing the influence of microwave damage etching on the breaking strength, extensive examinations on breakages were made *by customers*. For this purpose, blank silicon wafers (100) were halved after thinning and damage etching, and one half of a wafer was broken into approximately 50 pieces measuring around 12 by 12 mm^2 per test. The 50 pieces were then subjected to a breaking test, and the breaking force applied via a so-called Weibull-Plot. The respective other halfs of the wafers were used for SEM investigations and X-ray topological examinations.



g. 3: Damage etching with Microwave Downstream Plasma; Bow (µm) in dependence of grinding method, etch chemistry and etching time

The results show that even after 1 min etch time with the microwave downstream plasma on a SF_6-base, the breaking strength has doubled, after 2 min values over 2000 MPA are already reached for S_o. Then S_o gradually goes into saturation to reach, after 3 to 4 min, breaking strengths, which match those after a wet chemical damage etch process (removal approx. 5 µm).

The same result is obtained with thinner grinded wafers (≤ 200 µm final thickness) which can be handled and processed easier when using a foil.

Even though the highest Si-etch rates and shortest bow removal times can be obtained with NF_3-chemistry, SF_6-chemistry shows better values regarding breaking strength and optical quality of the wafer backside. As it is by far the cheapest chemistry, this chemistry remains in the focus of attention.

As far as costs (appr. 10 cents./wafer) and results are concerned, CF_4-chemistry can also be considered, especially when a rough surface is desirable, e.g. to obtain better glue-ing on SOJ lead

frames or a better adhesion of the moulding mass for LOC-mounting due to an enlarged surface.

With X-ray topological examinations, the breakage-examinations could be confirmed in respect to the fact, that after approx. 1 to 1,5 min microwave damage etching, none of the diffraction images typical for a previous grinding process could be seen.

Since the wafers are not subjected to a "healing" tempering step, as mentioned before, a damage-free process such as the "remote" microwave CDE (Chemical Downstream Etch)-process, should be used.

As the wafer frontside is protected by the foil, the wafers could be transported face down and be etched in the conventional way, i.e. from above, in the chamber. Of course, an etch equipment in which mechanical handling of the thinly grinded wafers is gentle, is recommended. This, e.g., is the case, when the etch equipment is designed as a load-lock system, and the whole charge can be pumped down and vented, respectively, in the load-lock, while the other charge is being processed. This has been realised in the Secon wafer backside etcher XCD-240. The use of the chamber, developed for backside etching without photoresist frontside protection, has the advantage that the wafers remain in their natural position, i. e. face up, as the wafer backside is etched from below in the chamber (Fig 1).

Conclusion

A new chamber for wafer backside etching and damage removal without frontside protection has been developed and tested. The chamber has been attached to a MESC-compatible cluster tool. In a two-chamber configuration, a throughput of more than 40 wafers/h can be obtained for PBL-mask backside removal. The costs for this PBL-process are a fraction compared to conventional methods. The gain in cycle time for a 50 wafer lot is nearly half a day compared to the approach with frontside protection.

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